

### Department of Electrical and Electronics Engineering

#### COURSE MODULES OF THE COURSE TAUGHT FOR THE ODD SESSION OCT-FEB 2023-24

##### Course Syllabi with CO's

Faculty Name: <b>Mrs. Swathi C A</b>				Academic Year: <b>2023-24</b>				
Department: Electrical & Electronics Engineering								
Course Code	Course Title	Core/Elective	Prerequisite	Contact Hours				Total Hrs/ Sessions
				L	T	P	S	
<b>BEE 306A</b>	<b>Digital Logic Circuits</b>	<b>Elective</b>	<b>Basic Electronics</b>	<b>3</b>	<b>-</b>	<b>-</b>	<b>-</b>	<b>40 Hr Theory</b>
<b>Objectives</b>	<ul style="list-style-type: none"><li>• To illustrate simplification of algebraic equations using Karnaugh Maps and Quine-McClusky methods</li><li>• To design decoders, encoders, digital multiplexer, adders, subtractors and binary comparators</li><li>• To explain latches and flip-flops , registers and counters</li><li>• To analyze Melay ad Moore Models</li><li>• To develop state diagrams synchronous sequential circuits</li><li>• To understand the applications of sequential circuits</li></ul>							
	<b>Topics Covered as per Syllabus</b>							
<b>Module-1 :</b> <b>Principles of Combinational Logic:</b> Definition of combinational logic, canonical forms, Generation of switching equations from truth tables, Karnaugh maps-3,4,5 variables, Incompletely specified functions (Don't care terms) Simplifying Max term equations, Quine-McCluskey minimization technique, Quine-McCluskey using don't care terms, Reduced prime implicants Tables. <b>Bloom's Taxonomy level: L<sub>1</sub> – Remembering; L<sub>2</sub> – Understanding; L<sub>3</sub> – Applying; L<sub>4</sub> - Analysing</b>								
<b>Module -2:</b> <b>Analysis and Design of Combinational logic:</b> General approach to combinational logic design, Decoders, BCD decoders, Encoders, digital multiplexers, Using multiplexers as Boolean function generators, Adders and subtractors, Cascading full adders, Look ahead carry, Binary comparators. <b>Bloom's Taxonomy level: L<sub>1</sub> – Remembering; L<sub>2</sub> – Understanding; L<sub>3</sub> – Applying; L<sub>4</sub> - Analysing</b>								
<b>Module-3:</b> <b>Flip-Flops:</b> Basic Bistable elements, Latches, Timing considerations, The master-slave flip-flops (pulsetriggered flip-flops): SR flip-flops, JK flip-flops, Edge triggered flip- flops, Characteristic equations <b>Bloom's Taxonomy level: L<sub>1</sub> – Remembering; L<sub>2</sub> – Understanding</b>								
<b>Module -4:</b> <b>Flip-Flops Applications:</b> Registers, binary ripple counters, synchronous binary counters, Counters based on shift registers, Design of a synchronous counter, Design of a synchronous mod-n counter using clocked T, JK, D and SR flip-flops. <b>Bloom's Taxonomy level: L<sub>1</sub> – Remembering; L<sub>2</sub> – Understanding; L<sub>3</sub> – Applying; L<sub>4</sub> - Analysing</b>								
<b>Module-5:</b> <b>Sequential Circuit Design:</b> Mealy and Moore models, State machine notation, Synchronous Sequential circuit analysis, Construction of state diagrams, counter design. Memories: Read only and Read/Write Memories, Programmable ROM, EPROM, Flash memory. <b>Bloom's Taxonomy level: L<sub>1</sub> – Remembering; L<sub>2</sub> – Understanding; L<sub>3</sub> – Applying; L<sub>4</sub> - Analysing</b>								
<b>List of Text Books</b>								
(1) Digital Logic Applications and Design, John M Yarbrough, Thomson Learning 2001 ISBN 981- 240-062-1. (2) Digital Principles and Design Donald D. Givone McGraw Hill 2002 ISBN 978-0- 07-052906-9. (3) Digital Design, Morris Mano, Prentice Hall of India, Third Edition. (4) Fundamentals of logic design. Charles H Roth, Jr. Cengage Learning. Fifth Edition.								

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List of URLs, Text Books, Notes, Multimedia Content, etc	
<ol style="list-style-type: none"> <li>1. <a href="http://www.nptel.ac.in/courses/106108099/Digital%20Systems.pdf">http://www.nptel.ac.in/courses/106108099/Digital%20Systems.pdf</a></li> <li>2. <a href="https://www.youtube.com/watch?v=VnZLRrJYa2I">https://www.youtube.com/watch?v=VnZLRrJYa2I</a></li> <li>3. <a href="http://nptel.ac.in/courses/117108040/downloads/Digital%20System%20Design.pdf">http://nptel.ac.in/courses/117108040/downloads/Digital%20System%20Design.pdf</a></li> <li>4. <a href="http://nptel.ac.in/courses/117105080/">http://nptel.ac.in/courses/117105080/</a></li> </ol>	
<b>Course Outcomes</b>	<p>At the end of the course the students will be able to:</p> <ol style="list-style-type: none"> <li>1. Develop simplified switching equation using Karnaugh Maps and Quine McClusky techniques.[L3]</li> <li>2. Apply the design procedures for Multiplexer, Encoder, Decoder, Adder, Subtractors and Comparator as digital combinational control circuits.[L3]</li> <li>3. Illustrate the design of flip flops and development of its characteristic equation.[L2]</li> <li>4. Apply the design procedures for counters and shift registers as sequential control circuits.[L3]</li> <li>5. Develop Mealy/Moore Models and state diagrams for the given clocked sequential circuits and Interpret the functioning of Read only and Read/Write Memories, Programmable ROM, EPROM and Flash memory.[L3]</li> </ol>
Internal Assessment Marks: 50 (2 Theory Tests of 25Marks each + 2 Assignments of 10 Marks each are conducted during the semester and marks allotted based on average all the performances).	

### The Correlation of Course Outcomes (CO's) and Program Outcomes (PO's)

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Course Code:	BEE306A	TITLE: Digital Logic Circuits						Faculty Name:	Ms. Swathi C A					
List of Course Outcomes	Program Outcomes													
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO-1	3	2	2	-	2	-	-	-	-	-	-	-	2	-
CO-2	3	3	2	-	2	-	-	-	-	-	-	-	2	-
CO-3	2	2	2	-	-	-	-	-	-	-	-	-	2	-
CO-4	2	2	2	-	-	-	-	-	-	-	-	-	2	-
CO-5	3	3	2	-	-	-	-	-	-	-	-	-	2	-

**Note:** 3 = Strong Contribution    2 = Average Contribution    1 = Weak Contribution    '-' = No Contribution